-- Often, several iterations of the design, layout, and testing process are required in order to optimize the semiconductor chip's size, cost, heat output, speed, power consumption, and electrical functionalities. However, one problem is attributable to the fact that each of these stages is highly dependent on the results of the other stages. A minor alteration in one stage intended to enhance one characteristic may cause unforeseen problems to occur in other stages. For example, changing a cell in the synthesis stage might drastically alter the current place and route. It is this high degree of interdependence which makes it extremely difficult to predict and account for the consequences associated with any changes. Indeed, the overall design might sometimes be worse in a successive iteration. Furthermore, the iterative process is time-consuming and requires a powerful computer to perform the processing. In addition, the iterative process is labor intensive and requires the dedication of a highly skilled, experienced EDA specialist. --

D1

2. Please replace the second paragraph on page 12 beginning with "The mapped netlist is input...", with the following paragraph:

-- The mapped netlist is input to a cell separator. Cell separation is then performed in step 306 to assign (x,y) coordinates for each cell in the mapped netlist 305. As described above, the task of cell separation is to calculate the positions of the cells. Since the quality of the placement determines the minimal achievable area and wiring length of a circuit, placement has a large impact on production yield and circuit performance. Cell separation tools handle the problem of assigning locations to cells (e.g., objects or

D2 Cont

elements) so as to minimize some overall cost function. In this area, the cost function is related to the wiring distance between cells. Cells must be assigned locations so that they do not overlap each other, they all fit within some overall bounding figure, and the total wiring cost is minimized. The output from cell separation process 306 is a number of cells, each of which has an assigned (x,y) position 307 denoting the approximate centerpoint of the cell. A subroutine call is made back to the synthesis program with the new cell location information 307. Based on this new cell information, the synthesis program then generates a new netlist 309. The (x,y) location of the cells 307 and the new netlist 309 are input to a spacing tool. The spacing step 310 changes the partition walls in order to improve the spacings between the cells. The updated partition wall locations 311 are generated by spacing step 310. Next, the updated partition walls 311 and the new netlist 309 are used to formulate new partitions in step 312. There are a number of different partitioning approaches that can be implemented with the present invention. One such method is disclosed in the article by Ren-Song Tsay, Ernest S. Kuh, and Chi-Ping Hsu, *PROUD: A Fast Sea-Of-Gates Placement Algorithm*, published in the 25th ACM/IEEE Design Automation Conference (1988), paper 22.3. This approach takes advantage of inherent sparsity in the connectivity specification for an integrated circuit design and solves repeatedly sparse linear equations by the SOR (successive over-relaxation) method in a top-down hierarchy. Another approach is disclosed in a paper by Alfred E. Dunlop and Brian W. Kernighan, *A Procedure for Placement of Standard-Cell VLSI Circuits*, published in the IEEE Transactions on Computer-Aided Design, Vol. CAD-4, No. 1, Jan. 1985. This approach is based on graph partitioning to identify groups of modules that ought to be close to each other, and uses a technique for properly accounting for external connections at

D2 Cont

D